

CLAIMS:

1. A memory card having a plurality of non-volatile memories and a memory controller for controlling operation of said non-volatile memories, wherein

said memory controller performs an access control of said non-volatile memories in response to an external access instruction, and an alternation control for alternating a storage area of an access error-related non-volatile memory with other storage area;

said memory controller causes said plurality of non-volatile memories to operate for parallel access in said access control; and

said memory controller makes the storage area alternative in unit of the non-volatile memory in which an access error occurs in said alternative control.

2. A memory card having a first and second non-volatile memories and a main controller for controlling operation of said non-volatile memories, wherein

said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data, respectively;

said memory controller causes said first and second non-volatile memories to operate for parallel access in an access control of said non-volatile memories in response to an external access instruction; and

said memory controller makes storage areas

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alternative in unit of the non-volatile memory in which an access error occurs, in an alternation control for alternating a storage area of the access error related non-volatile memory with other storage area.

3. A memory card as defined in Claim 1, further comprising buses for connecting respective non-volatile memories to said memory controller so that said respective non-volatile memories are separately access-controlled.

4. A memory card as defined in Claim 1, wherein said memory controller includes an ECC circuit for adding an error detection code to write-data written into said non-volatile memory to conduct an error detection and correction for read-data from said non-volatile memory; and

said ECC circuit conducts an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

5. A memory card as defined in Claim 1 wherein said memory controller includes one or more ECC circuits which add an error detection code to write-data written into said non-volatile memory to conduct an error detection and correction for read-data from said non-volatile memory, said ECC circuits being as many as the number of the parallel access operations; and

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said ECC circuit performs input/output operations in a parallel manner at an operation frequency which is equal to the input/output operation frequency of said parallel access operated non-volatile memories.

6. A memory card having a plurality of non-volatile memories, a control circuit for controlling operation of said non-volatile memories, and an ECC circuit for adding an error detection code to write-data written into said non-volatile memories to perform error detection and correction for read-data from said non-volatile memories, wherein

said control circuit causes said plurality of non-volatile memories to parallel access operate in an access control of said non-volatile memories responsive to an external access instruction; and

said ECC circuit performs an input-output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of said parallel operations.

7. A memory card having a plurality of non-volatile memories, a control circuit for controlling operation of said non-volatile memories, and an ECC circuit for adding an error detection code to write-data written into said non-volatile memories to conduct error detection and correction for read-data from said non-volatile memories, wherein

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said control circuit causes said plurality of non-volatile memories to parallel access operate in an access control of said non-volatile memories responsive to an external access instruction; and

each of said ECC circuits performs an input-output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories.

8. A memory controller comprising:

a host interface circuit capable of being input/output operated in accordance with a predetermined protocol;

a memory interface circuit capable of be connected to a plurality of non-volatile memories in parallel; and

a control circuit connected to said host interface circuit and said memory interface circuit, wherein

said control circuit performs an external interface control via said host interface circuit, an access control of said non-volatile memories via said memory interface circuit responsive to an external access instruction, and an alternation control for alternating an storage area of an access error related non-volatile memory with other storage area, causes said plurality of non-volatile memories to parallel access operate in said access control, and makes the storage areas alternative in unit of the non-volatile

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memory in which an access error occurs, in said alternate control.

9. A memory controller comprising:

a host interface circuit capable of being input/output operated in accordance with a predetermined protocol;

a memory interface circuit capable of being connected to first and second non-volatile memories in parallel; and

a control circuit connected to said host interface circuit and said memory interface circuit, wherein

said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data, respectively, causes said first and second non-volatile memories to parallel access operate in an access control of said non-volatile memories in response to an external access instruction, and makes storage areas alternative in unit of the non-volatile memory in which an access error occurs, in an alternate control for alternating a storage area of the access error related non-volatile memory.

10. A memory controller as defined in Claim 8, further comprising an ECC circuit for adding an error detection code to write-data written into said non-volatile memory to perform an error detection and correction for read-data from said non-volatile memory,

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wherein

said ECC circuit performs an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

11. A memory controller as defined in Claim 8 further comprising an ECC circuit for adding an error detection code to write-data written into said non-volatile memory to perform an error detection and correction for read-data from said non-volatile memory, wherein

said ECC circuit performs an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of said parallel access operation.

12. A memory controller as defined in Claim 8, wherein said memory controller is formed on one semiconductor chip.

13. A memory card comprising:
a control circuit;
a plurality of non-volatile memories;
an external interface circuit connected to an external device; and
a bus, wherein
said plurality of non-volatile memories have a plurality of input/output terminals;

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said bus has a first bit width, is divided into each of bits having a predetermined number, and is connected to the input/output terminal of corresponding one of said non-volatile memories; and

said control circuit performs an access control to said plurality of non-volatile memories, and performs address alternating processing for each of said non-volatile memories when an access error occurs in an access to the non-volatile memories.

14. A memory card comprising:
a control circuit;
a plurality of non-volatile memories;
n error detection and correction circuits, n being an integer which is one or more; and
a bus, wherein

said control circuit performs an access control to said plurality of non-volatile memories;
each of said plurality of non-volatile memories has an input/output terminal with a first bit width $W1$, and can be accessed at an access frequency $F1$;

said bus has a bit width of $W1 \times m$, and is connected to the input/output terminals of m non-volatile memories in parallel;

said error detection and correction circuits can detect and correct an error of data with a bit width $W2$;

an operation frequency $F2$ of said error

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detection and correction circuits is represented as follows;

$$F2 \geq (F1 \times W2 \times m) / (W2 \times n).$$

15. A memory controller comprising:

a control circuit;

an input/output terminal with a first bit width; and

one or more error detection and correction circuit, wherein

said error detection and correction circuit conducts error correction of data which is input and output via said input/output terminal; and

said control circuit has an address alternating capability, controls input/output of data via said input/output terminal, and when an access error occurs in the input/output of data at an address, divides said input/output terminal into groups each having a second bit width to alternate an address in a group, in which an access error occurs, with other address.

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